REMARKS

Claims 1-14 and 16-30 are pending. The independent claims included in claims 1-14 and 16-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by Meizlik (6,112,323). Dependent claims 13, 14, and 17-20 were rejected under 35 U.S.C. 103(a) as being unaptetnable over Meizlik. Dependent claims 4, 16, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Meizlik in view of Malek (5,086,467). The Examiner relied on Meizlik to reject all independent claims.

Meizlik describes a computer network. "When a message, such as message 106, is to be transmitted it is passed to a component which is responsible for sending the message using the appropriate mechanisms. Thus, embodiments within the scope of the present invention may comprise means for sending a message. By way of example, and not limitation, in FIG. 6 such means is illustrated by sender 108. Sender 108 is responsible for sending all of the packets in a message. In addition, when using the statistical reliability mode sender 108 is also responsible for ensuring that the required minimum number of transmission packets are produced when message 106 is sent. This is illustrated in FIG. 6 by packets 110 which are transmitted over network 112 to recipients 114. Recipients 114 represent one or more intended recipients of the message. Throughout the application, it should be appreciated that the protocols described herein may be used between any sending system and one or more receiving systems. In one embodiment, sender 108 is incorporated into a short message send/receive facility, such as short message send/receive facility 66 of FIG. 3. Also as illustrated in FIG. 3, sender 108 may rely on a protocol stack including various hardware components, hardware drivers, and other protocol drivers to transmit the packets. As previously described above, in one embodiment packets 110 may conform to those illustrated in FIG. 5." (Meizlik Figure 6 description)

Athough Meizlik does describe a pseudo random number generator, Meizlik does not teach or suggest a variety of elements recited in the claims. Meizlik does not teach or suggest arbitration logic, a primary component, and a secondary component as recited in independent claims 1, 21, and 28 or an interconnection module, a primary component, and a secondary component as recited in independent claim 13.

Independent claims 1, 21, and 28 all recite arbitration logic, a primary component, and a secondary component. It is recognized that the Examiner is reading the claims in their broadest

possible light. However, even with a broad reading, Meizlik does not teach or suggest arbitration logic, a primary component, and a secondary component. The Examiner argues that a message handler 160 of Figure 8 in Meizlik is arbitration logic. The message handler 160 sits between a message receive list 150 and an application 142. The message handler 160 appears to "pass the message to the application." (column 26, lines 41-43) The message handler 160 is not arbitration logic and performs no arbitration. At most, the message handler 160 may perform some processing on a message prior to passing the message to the application. This directly contrasts with the "arbitration logic" recitation in the claims.

According to various embodiments, particular examples of arbitration logic are a slave side arbitration bus and an AvalonTM bus fabric. "Logic and mechanisms for providing the control signal based on criteria such as fairness or priority are referred to herein as arbitration logic. The inputs of the arbitrator switching circuitry 261 and 263 are connected to primary CPU 213 and primary Ethernet 215. The outputs of the arbitrator switching circuitry 261 and 263 are connected to secondary UART 221, secondary PIO 223, and secondary memory 225. The outputs of the secondary components transmit information such as read data back to the primary components through a decoder 209. A mechanism for selecting secondary components and translating control information such as addresses is referred to herein as a decoder. In conventional computer systems, there is a single decoder for each bus. A decoder 209 includes decoder logic 203 and decoder switching circuitry 265 for selecting the particular secondary component data transfer. A decoder can also be referred to as a primary side arbitrator including primary side arbitration logic and primary side switching circuitry." (page 9, line 27 - page 10, line 7)

Meizlik also does not teach or suggest a primary component or a secondary component. The Examiner argues that primary component is a sender and a secondary component is a receiver. The Applicants respectfully disagree. As will be appreciated by one of skill in the art and as explicitly defined in the specification, a primary component is also referred to as a master component and a secondary component is also referred to a slave component. A mere sender and a receiver are not primary and secondary components.

According to particular embodiments, a "component or device that is operable to initiate read and/or write operations by providing control information is referred to herein as a primary component. Primary components are sometimes referred to as master components. Control

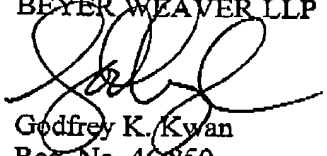
information can include a particular address associated with a secondary component. Any component or device that responds to read or write operations with information sent back to the primary component regarding the read or write operation is referred to herein as a secondary component. Secondary components are sometimes referred to as slave components. Some examples of primary components are processors, microcontrollers, and Ethernet devices. Some examples of secondary components are Universal Asynchronous Receiver Transmitters (UARTs), Parallel Input Output (PIO), program memory, and data memory. It should be noted that some components such as an Ethernet component can be both a primary component and a secondary component, as an Ethernet component has the capability of reading and writing to the secondary program memory while also responding to instructions from a primary system CPU." (page 9, lines 11-25)

Furthermore, even if the Examiner somehow broadly interprets primary component to be a sender and a secondary component to be a receiver, the message handler that the Examiner argues is arbitration logic does not couple the sender 144 to the receiver 148 (e.g. see Figure 8). The arbitration logic merely resides between a message receive list 150 and an application 142. It is respectfully submitted that the message receive list 150 and the application 142 are not primary and secondary components either. Furthermore, it is respectfully submitted that a message handler is also not an interconnection module.

Although the claims are believed allowable in their current form, claim 21 is being amended to clarify aspects of the invention. Claim 21 now recites "wherein the plurality of primary components are master components on the programmable chip" and "wherein the plurality of secondary components are slave component on the programmable chip." None of the references cited is believed to teach or suggest these recitations.

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER LLP



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